## Remarks

The following numbered paragraphs are provided to respond to the similarly numbered paragraphs in the Office Action (e.g., paragraph "1" below corresponds to paragraph 1 in the Office Action.

1. Applicant recognizes that prior art must be identified on a 1449 form to be considered by the Examiner. Applicant notes that the patents indicated in the current specification were simply to teach general background information and are not material to the claimed invention and therefore have not been submitted on a 1449 form.

2. Applicant has amended the drawings as suggested by the Examiner.

3. Applicant has amended the drawings so that each of the EDPs is referenced by a number followed by a capital "I" (e.g., 5I, 2I, etc.). In addition, Applicant has amended the specification so that the EDP labels in the specification are consistent with the labels in the Figures.

4. Applicant has amended the specification to eliminate the reference to table 13.

5. Applicant has amended the specification so that the identified reference numbers are referred to therein. The reference numeral 23 has been removed from Fig. 1.

6. Applicant has amended the specification as suggested by the Examiner.

7. Claims 17 and 20 have been amended as suggested by the Examiner.

8-9. Applicant has considered the inventorship issue and believes inventorship in this case remains correct.

10. The Office Action rejected each of claims 1, 2, 4-8, 10-12, 17, 19 and 20 as obvious over Mertens in view of allegedly admitted prior art. Applicant traverses this rejection.

With respect to paragraph 57, paragraph 57 teaches something completely different than extending master clock cycles as required by the originally filed claims. To this end, while paragraph 57 indeed stated that current technology already delays signals that occur during one master clock cycle so that they are processed as having occurred during a following clock cycle, delaying signals in this fashion does not alter the length of the master clock cycles (i.e., does not result in extended cycles).

When delays like the processing delays discussed in paragraph 57 are applied, the delays are applied in the same fashion to all of the EDP Q signals so that, while all of the Q signals that occur during the last 64 nsec. (i.e., the delay in the example in the specification was 64 nsec.) of a first master clock cycle will be shifted into a second master clock cycle that follows the first, a similar number of Q signals that occur during the last 64 nsec. of the second master clock cycle will be shifted into a third master clock cycle that follows the second and a similar number of Q signals that occur during the last 64 nsec. of the third master clock cycle will be shifted into a fourth master clock cycle, and so on. Thus, while Q signals are shifted from one master clock cycle to the next, the durations of the clock cycles are not altered (i.e., a 250 nsec. clock cycle remains 250 nsec. despite shifting of Q signals).

For a better understanding of why Q signals have been shifted in the past refer to Fig. 3 of the present specification and associated text at the end of paragraph 43. In Fig. 3, signals on lines 26 propagate through the illustrated circuitry along two general paths, a first through identifier 220 and a second through TPC 68 and converter 56/module 222. In many cases the propagation times through the first and second paths are different. For instance, in the exemplary case described in paragraph 43 it is assumed that the propagation time difference is 64 nanoseconds (i.e., the processing time along the path through identifier 220 is 64 nsec. greater than the processing time along the other path through converter 56/module 222).

Despite the propagation time difference, the signals provided to circuitry 200 have to be re-sinced prior to processing by circuitry 200. Where the propagation delay is 64 nsec. the signals can be re-sinced by delaying the path through converter 56/module 222 by 64 nsec. (see, in this regard, paragraph 43, lines 7-9 that states "Thus, for instance, in some cases each EDP Q will be delayed for tens of

nanoseconds (e.g., 64 nsec.) so that a delayed signal Q is provided to converter 56 and module 222").

Thus, in the above example, all Q signals are delayed by 64 nsec. such that a portion (e.g., approximately one fourth) of the Q signals that occur during each of the master clock cycles are shifted into the next clock cycle. Again, here, Applicant notes that equal shifting among master clock cycles does not change the durations of the clock cycles.

Turning to the claims, claim 1 requires, among other things, adding an overlapping period to a second master clock cycle to generate an extended cycle. Each of claims 7 and 17 include similar limitations. Mertens fails to teach or suggest extending clock cycles. As indicated above the present specification does not admit that extending cycles is taught by the prior art but rather teaches that systems exist wherein all Q signals are equally delayed which does not result in longer or extended clock cycles. For at least this reason Applicant believes that each of claims 1, 7 and 17 and claims that depend therefrom are patently distinct over the cited references and admitted prior art and requests that the rejection be withdrawn.

11. Applicant thanks the Examiner for allowing claims 13-16.

12. Applicant has not amended claims 3, 9 and 16 as Applicant believes that the original independent claims are patentable as described above.

Applicant has introduced no new matter in making the above amendments and antecedent basis exists in the specification and claims as originally filed for each amendment. In view of the above amendments and remarks, Applicant believes claims 1-20 of the present application recite patentable subject matter and allowance of the same is requested. No fee in addition to the fees already authorized in this and accompanying documentation is believed to be required to enter this amendment, however, if an additional fee is required, please charge Deposit Account No. 07-0845 in the amount of the fee.

Respectfully submitted,

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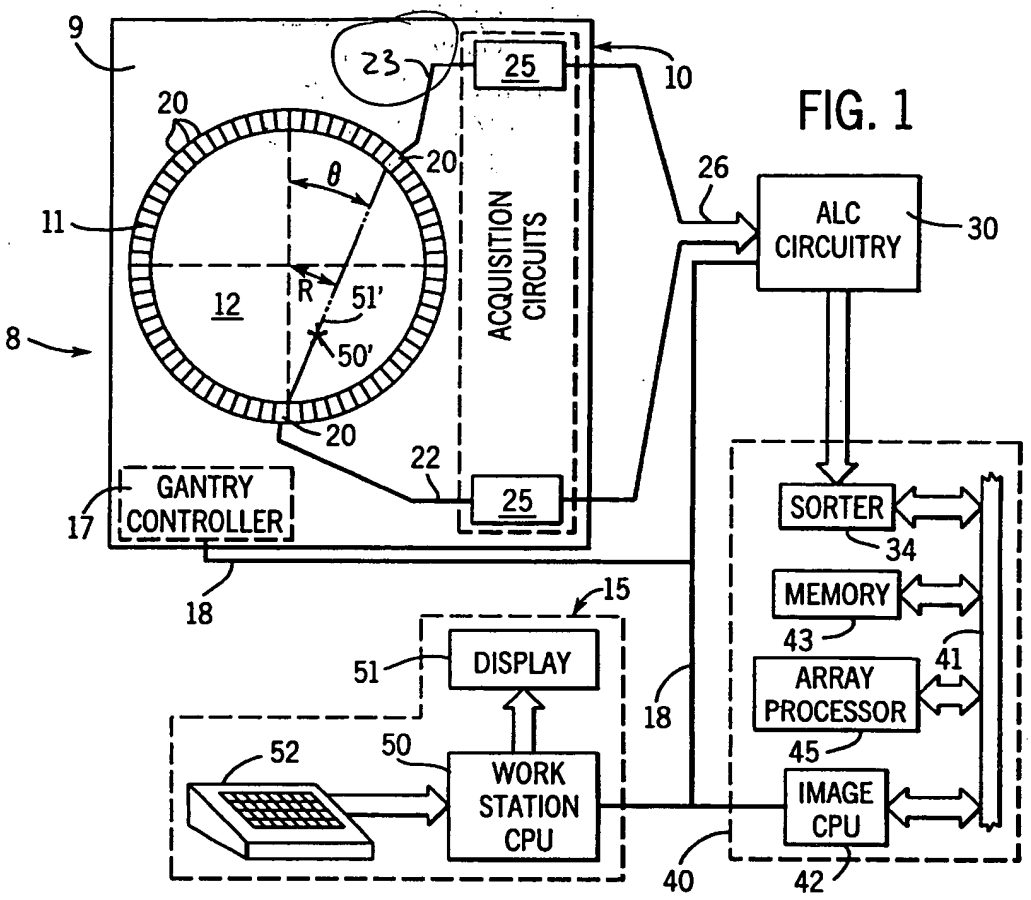


FIG. 1

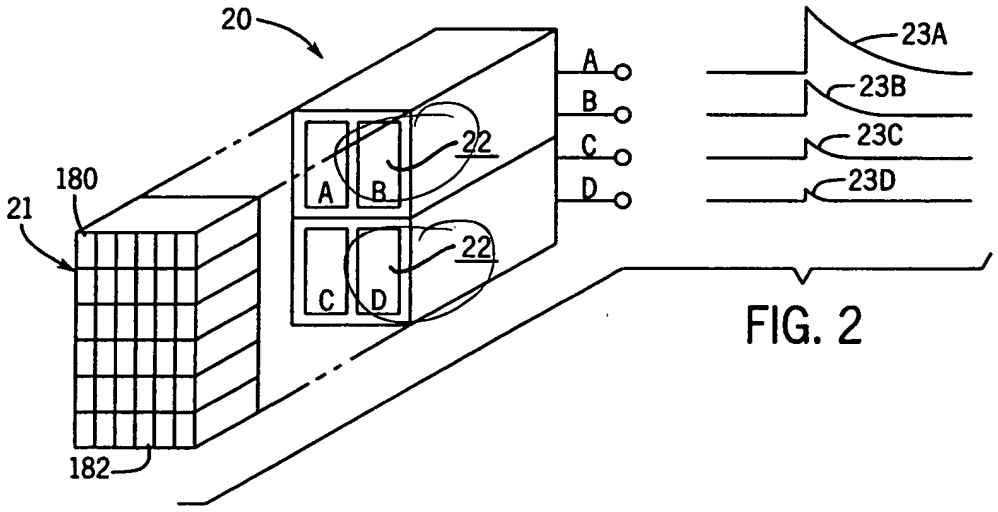


FIG. 2

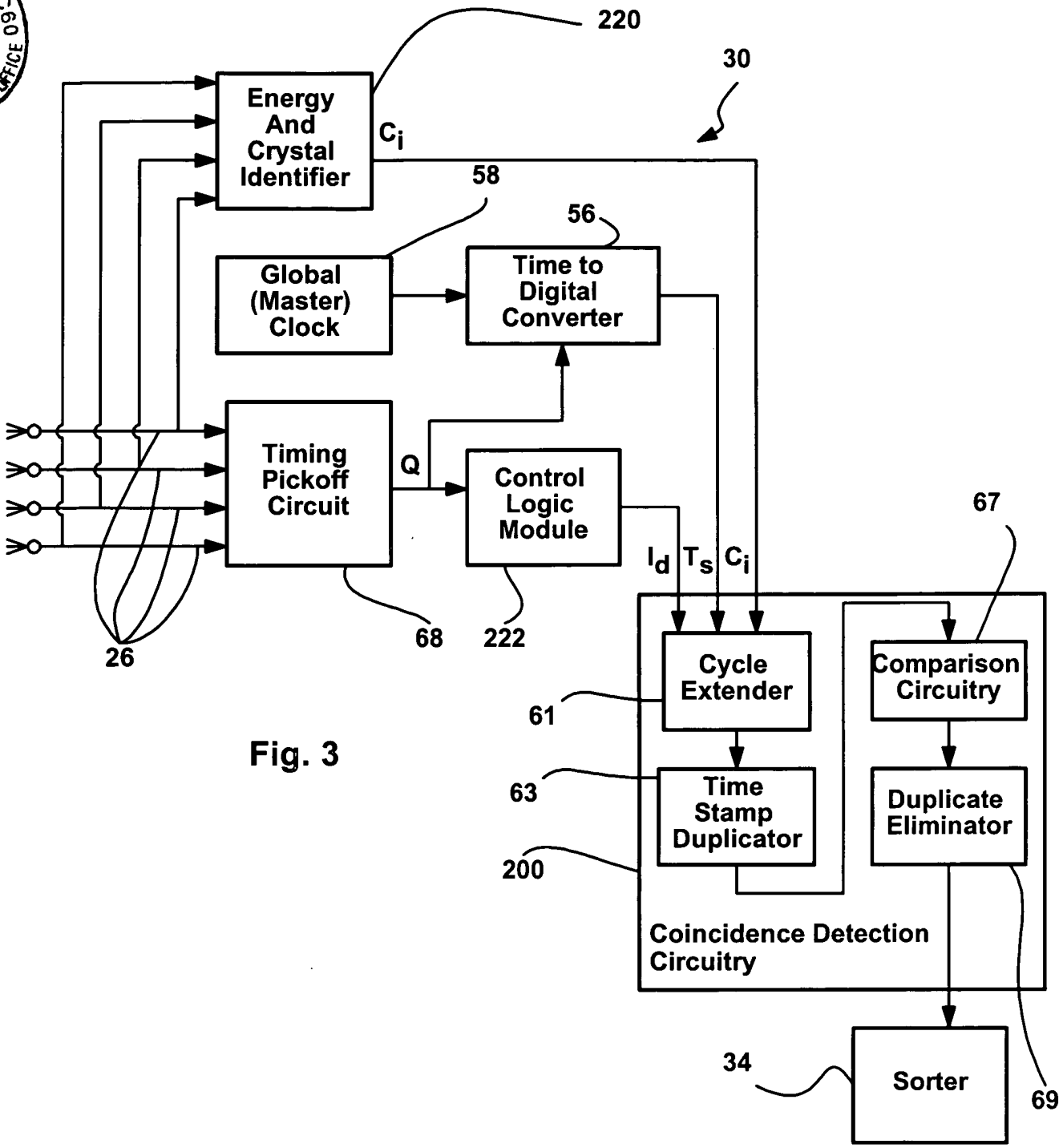


Fig. 3

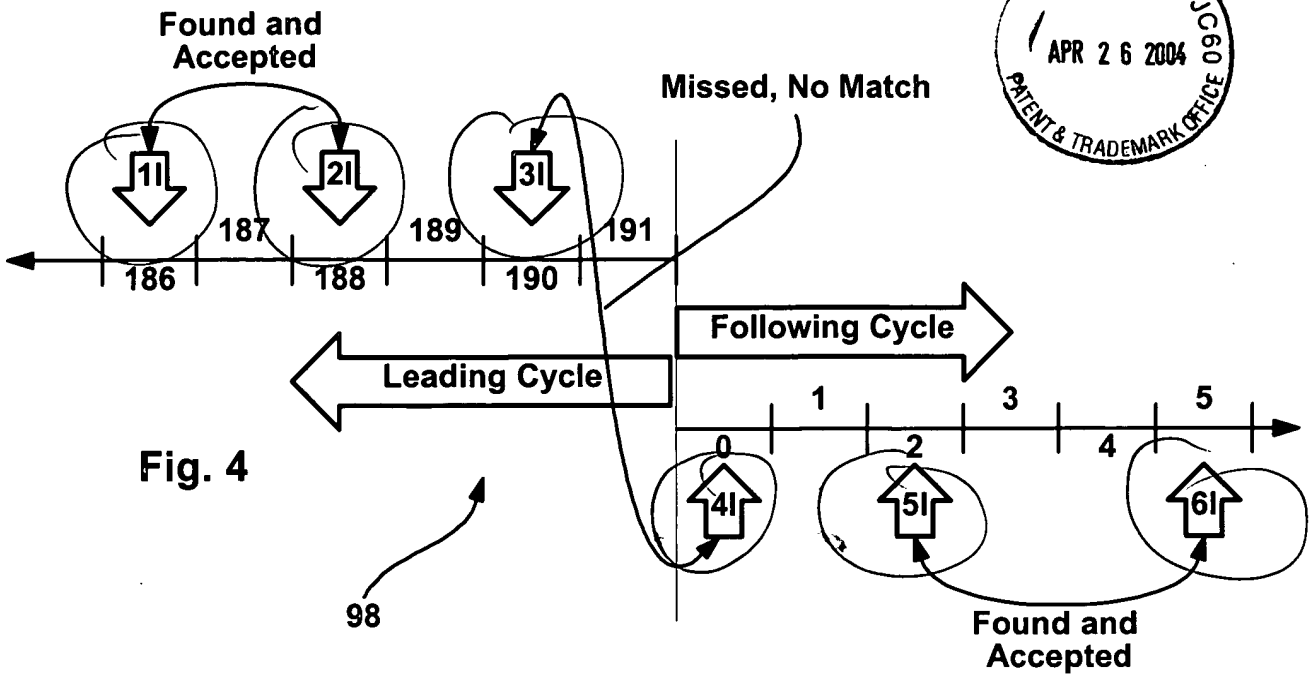


Fig. 4

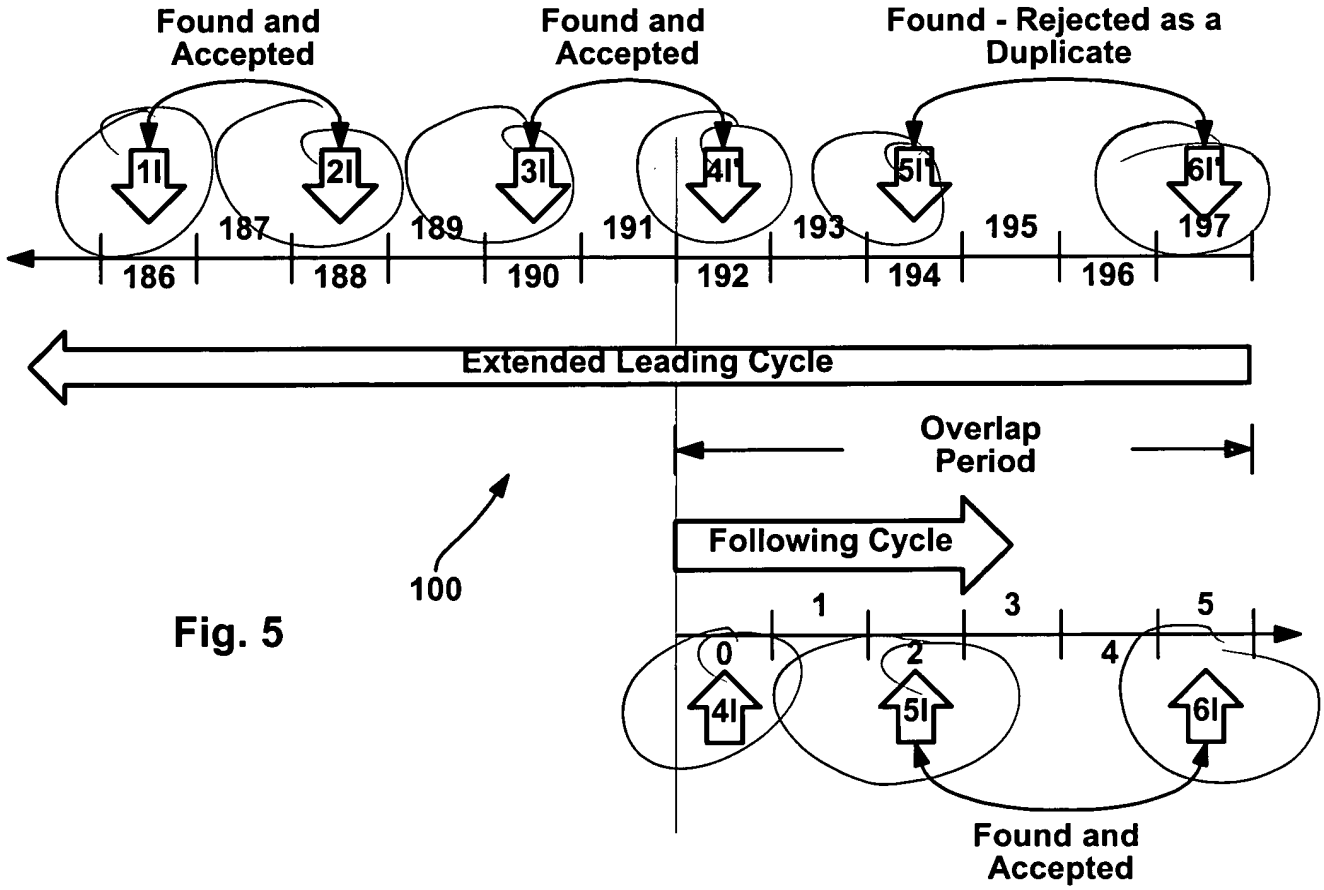


Fig. 5

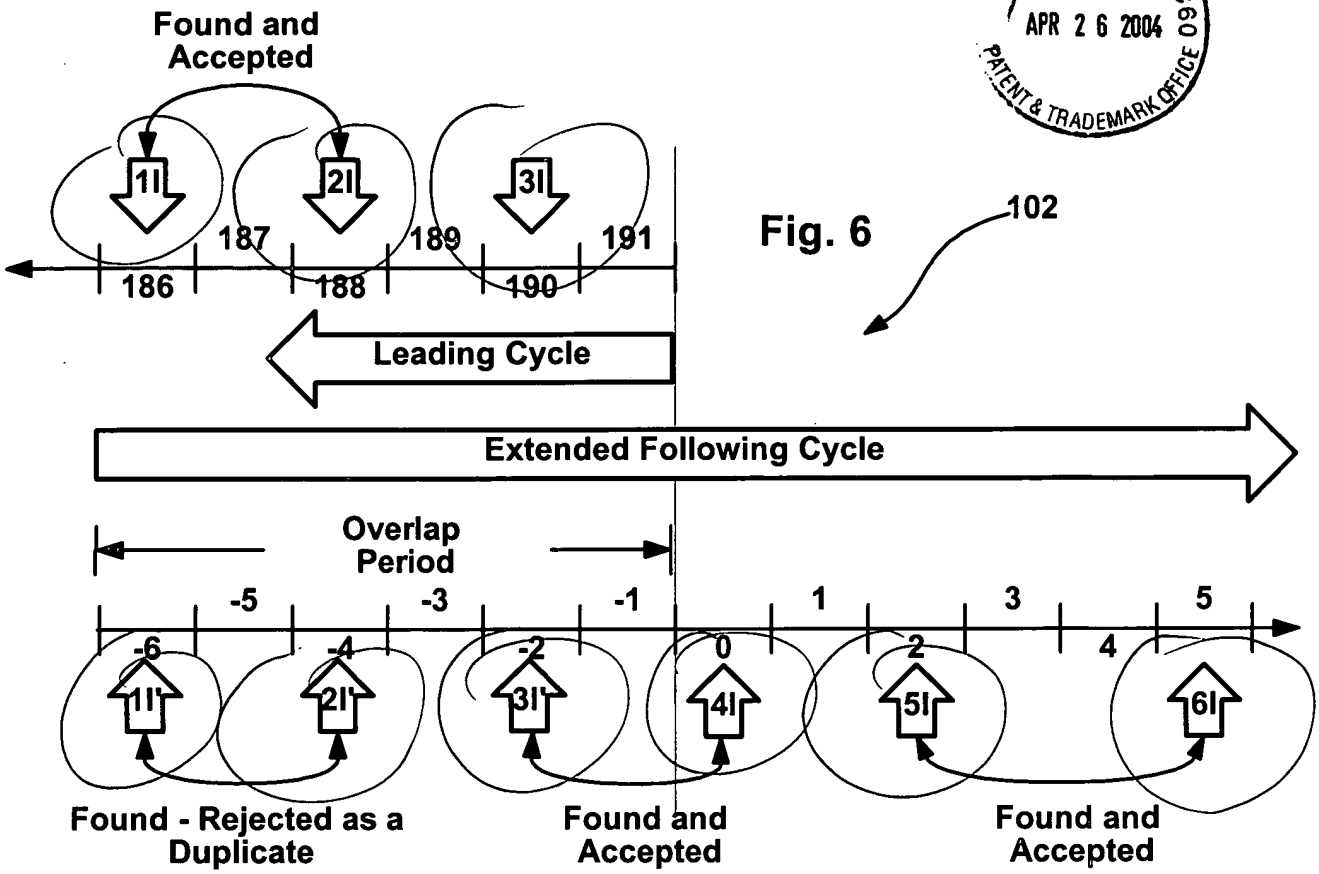


Fig. 6

Fig. 7